IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IV. Remarks

Rejection of Claims 2 and 20 Under 35 U.S.C. §112, Second Paragraph.

Applicant has amended claims 2 and 20 to recite items that are "aligned... in a second direction" and "aligned... in a first direction", respectively. These amendments are believed to address any perceived ambiguity in the term "linearly aligned".

Rejection of Claim 1 Under 35 U.S.C. §112, Second Paragraph.

Applicant has amended claim 1 to recite "adjacent". Applicant believes that this term, particularly in light of the additional amendments to this claim clearly define the metes and bounds of the invention.

Rejection of Claims 8 and 14-15 Under 35 U.S.C. §112, Second Paragraph.

Claims 8 and 14-15 have been amended to address this ground for rejection.

Rejection of Claims 1-21 Under 35 U.S.C. §103(a) based on Applicant's Background Art (*BACKGROUND ART*) in view of U.S. Patent No. 5,307,381 (*Ahuja*).

The rejection of claims 1-14 will first be addressed.

The invention of amended claim 1 is directed to a memory controller connected to a semiconductor memory device. The memory controller includes a clock generating circuit, a data generating circuit, a predetermined number "m" data output terminals, m output holding circuits, a predetermined number "n" signal output terminals that provide output strobe signals to the semiconductor memory device in synchronism with the output data, where $n < m$. Also included is a plurality of output delay circuits including one output delay circuit for every "p" signal output terminal(s), where p is an integer greater than zero. Each output delay circuit delays the output clock signal by a predetermined amount to transmit an output strobe signal to the corresponding p signal output terminal(s). The memory controller further includes a circuit core region in which the clock generating circuit and data generating circuit are formed, and an interface region surrounding the circuit core region in which the data output terminals, output holding circuits, signal output terminals, and output delay circuits are formed. Each m output holding circuit is adjacent to a corresponding one of the m data output terminals in a first

direction between the corresponding data output terminal and the circuit core region. An output of each output delay circuit is adjacent to the corresponding p signal output terminal(s) in the first direction between the corresponding signal output terminal and the circuit core region.

As is well settled, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

As emphasized above, Applicant's amended claim 1 recites "an output of each output delay circuit is adjacent to the corresponding p signal output terminal(s) in the first direction between the corresponding signal output terminal and the circuit core region". The above limitation is not believed to be shown or suggested by the cited reference.

As noted by the rejection, Applicant's *BACKGROUND ART* does not teach a plurality of delay circuits:

> Applicant's *[BACKGROUND ART]*... does not mention "a plurality of output delay circuits." (Office Action, dated 08/14/2006, Page 14, Lines 3-5).

To show such claim limitations the rejection appears to rely on two different rationales. First, the rejection reasoning appears to take official notice:

> [I]t is well known... that every electronic circuit has a "fan-out" limitation... as the number of loads exceeds the "fan-out" (or driving) capability of a single circuit, a plurality of circuits must be used to ensure proper operations. (Office Action, dated 08/14/2006, Page 14, Lines 3-5).

If official notice is being taken, Applicant seasonably traverses such official notice and requests a reference in support.

In addition, it is noted that this proposed prior art teaching neither shows nor suggests any particular relationship between the position of a delay circuit output with respect to a corresponding signal output terminal. Accordingly, even if such a teaching is well known, Applicant does not believe that modifying the *BACKGROUND ART* according to such a teaching

can arrive at Applicant's particular claim 1 limitations, where an output of each output delay circuit is adjacent to corresponding p signal output terminal(s).

The second rationale relies on *Ahuja*:

> Ahuja discloses... a "length equalizer" [figure 1, 14; figures 3-4; column 7, lines 19-41]... The length equalizer... equalizes the length of all clock lines [figure 1, 31-40n] such that the delay for the clock signal on each of the clock lines is equal... (Office Action, dated 08/14/2006, Page 14, Lines 3-5).

First, Applicant must stress that *Ahuja* teaches a clock signal distribution network for an input clock signal:

> Clock signal distribution network 20 generates the clock signal CLK from the ***clock input signal*** INCLK and then applies the clock signal CLK to each of functional units UNIT1-UNITn. (*Ahuja*, Col. 5, Lines 16-18, emphasis added).

Applicant's claim 1 is directed to output delay circuits that delay an output clock signal. Thus, the proposed combination cannot arrive at Applicant's invention.

In addition, the above rejection rationale does not show or suggest Applicant's limitations with respect to the positioning of delay circuits. In fact, Applicant believes that *Ahuja* teaches away from Applicant's claim limitations.

Applicant's amended claim 1 recites "an interface region... in which the... output delay circuits are formed". Further, each delay circuit is "adjacent to the corresponding p signal output terminal(s) in the first direction between the corresponding signal output terminal and the circuit core region".

In contrast, *Ahuja* teaches length equalizer (argued to show Applicant's delay circuits) at a centralized location:

> Length equalizer 14 is, in the presently preferred embodiment, located within the area of global clock driver 13, ***which is the center area of microprocessor 10***. (*Ahuja*, Col. 6, Lines 49-52).

This is believed to teach away from Applicant's claim 1 limitations, in which delay circuits are formed in the interface region.

Accordingly, because the cited combination of references and/or proposed prior art teachings does not show or suggest all the limitations of claim 1, Applicant believes that a prima facie case of obvious has not been established, and this ground for rejection is traversed.

Various claims depending from claim 1 are believed to be separately patentable over the cited reference.

Amended claim 2, which depends from claim 1, recites that the "m output data output terminals and n signal output terminals are aligned with one another in a second direction", "the m holding circuits are aligned with one another in the second direction", and the "output delay circuits are aligned with one another in the second direction between the m holding circuits and the m data output terminals and n signal output terminals".

To address this ground for rejection, Applicant incorporates by reference the same general comments set forth above for claim 1. Just as the cited combination of references/teachings does not show or suggest delay circuit output positions as noted in claim 1, such references/teachings do not show or suggest aligning such circuits in between, and in the same direction as, signal output terminals and holding circuits.

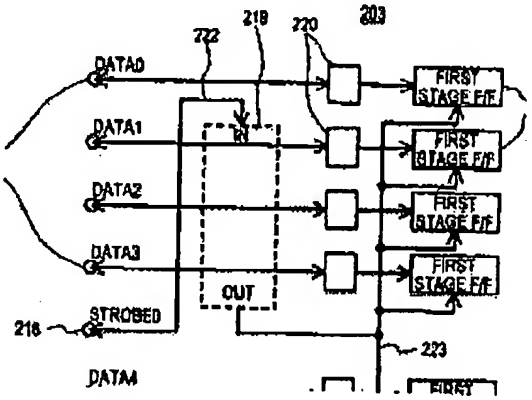
In particular, the proposed teachings regarding signal fan-out provide no suggestion as where buffer or delay circuits can be situated. As a result, such teachings cannot be suggestive of aligned output delay circuits, and an interface region in which such output delay circuits are formed. *Ahuja* teaches delay circuits, but such circuits are far away from clocked circuits (e.g., holding circuits) by being at a central location.

Accordingly, Applicant believes that a prima facie case of obviousness has not been established for this claim.

Amended claim 7, which depends from claim 1, recites a plurality of data input terminals, a signal input terminal for every "q" (where $q > 2$) data input terminals, and an input delay circuit corresponding to each signal input terminal. Each input delay circuit delays a received device input clock to generate an input strobe signal. Each input delay circuit has a circuit input position that is aligned with the corresponding signal input terminal in the first direction, and a circuit output position that is offset in the second direction with respect to the corresponding

signal input terminal. Also included is an input holding circuit corresponding to each data input terminal.

FIG. 11 of Applicant's *BACKGROUND ART* shows an arrangement with input delay circuits 219 corresponding to signal I/O terminals 216. However, as shown below, unlike Applicant's amended claim 7, the arrangement of the *BACKGROUND ART* appears to be the opposite of what is claimed.



Further, because of these considerable differences Applicant does not believe that the teachings of the *BACKGROUND ART* can be suggestive of Applicant's claim 7.

For this reason, claim 7 is believed to be separately patentable.

Claim 8, which depends from claim 1, recites a plurality of data input terminals, a signal input terminal for every "q" ($q > 2$) data input terminals, an input delay circuit corresponding to each signal input terminal, and an input holding circuit corresponding to each data input terminal. Also included is a first wiring corresponding to each data input terminal that transmits digital data to a corresponding input holding circuit, and a second wiring corresponding to each input holding circuit that transmits the input strobe signal from a corresponding input delay circuit to the input holding circuit. The first and second wiring corresponding to each input holding circuit are equal in length.

As emphasized above, claim 8 recites both a "first wiring... that transmits digital data" a "second wiring... that transmits the input strobe signal". Further, "first and second wirings corresponding to each input holding circuit are equal in length".

The rejection reasoning appears to rely on the *BACKGROUND ART* and/or *Ahuja* to

show such limitations.

With respect to the reasoning based on the *BACKGROUND ART*, Applicant believes that a prima facie cannot have been established, as it appears to be based on an erroneous interpretation of the art. The rejection reasoning argues first and second wirings are shown in the *BACKGROUND ART* according to the following reasoning:

> As to claim 8, Applicant's [*BACKGROUND ART*] teaches... ***a first wiring...that transmits digital data to a corresponding input holding circuit*** [figure 11, 2211]... ***a second wiring... that transmits the input strobe signal...*** [figure 11, ***2212***]... it is assumed that the plurality of wirings 225 can have the same length (paragraph 0017)... (Office Action, dated 08/14/2006, Page 17, Line 3 to Page 18, Line 9, emphasis added).

Applicant first notes that item 2212 of Applicant's *BACKGROUND ART* cannot be a "second wiring" as it <u>does not</u> transmit an input strobe signal, but rather transmits input data:

> ***Data input*** at data I/O terminals 215 is supplied to data delay circuits 220 through wirings 2211. After being skew-adjusted, such data is supplied to first stage FFs 217 ***through wirings 2212***. (Applicant's Specification, paragraph [0021], emphasis added).

Accordingly, the rejection reasoning relying on FIG. 11 of the *BACKGROUND ART* is in error, and thus cannot show or suggest a "second wiring" as claimed.

As shown in the above excerpt, the rejection reasoning also argues that wirings 225 of the *BACKGROUND ART* "have the same length". This is correct. However, wirings 225 can be neither a "first wiring" nor a "second wiring". Wirings 225 transmit data <u>from</u> a flip flop (FF) <u>to</u> an I/O terminal. That is, wirings 225 describe <u>output data signals</u>. This is the opposite of the first and second wirings, which are clearly <u>input signals</u>

> Final stage FFs 218 capture data from the data storing circuit 211... Such captured data is then ***supplied to data I/O terminals 215 through signal lines 225.***

(Applicant's Specification, paragraph [0021], emphasis added).

Accordingly the rejection reasoning relying on FIG. 10 of the *BACKGROUND ART* is also in error, and thus cannot establish a prima facie case of obviousness.

The rejection reasoning relying on *Ahuja* cannot establish a prima facie case as it cannot show or suggest a "first" and "second wiring" of equal length, as recited in claim 1. Applicant readily admits *Ahuja* shows clock wirings of equal length. However, the reference is utterly silent as to any teachings related making such a clock wiring equal in length to "a first wiring...that transmits digital data to a corresponding input holding circuit".

Accordingly, Applicant believes that claim 8 includes limitations not shown in or suggested by the combination of reference/teachings, and thus is separately patentable.

Amended claim 11, which depends from claim 1, is believed to be separately patentable for the same essential reason as claim 7. In particular, while the *BACKGROUND ART* shows an input delay circuit, such a circuit shows circuit input and circuit output positions essentially the opposite to that recited in amended claim 11.

Amended claim 14, which depends from claim 1 via claim 13, is also believed to be separately patentable for the same essential reason as claim 8. In particular, neither the *BACKGROUND ART* nor *Ahuja* show or first and second wirings of equal length, such teachings cannot show a first wiring having a length equal to a sum of second and third wiring.

The rejection of claims 15-21 will now be addressed.

The invention of claim 15 is directed to a memory controller connected to a semiconductor memory device that includes a predetermined number "m" data input terminals, a predetermined number "n" signal input terminals (where m > n), a data storing circuit for receiving digital data from the data input terminals. Also included are n input delay circuits that delay received device input clock signals from the semiconductor memory device, m input holding circuits that hold the input data in synchronism with the input strobe signals generated by the input delay circuits, and m data input wirings. Each data input wiring transmits an input data value from one data input terminal to a corresponding input holding circuit. The memory controller further includes m signal input wirings transmitting one input strobe signal from one

input delay circuit to a corresponding input holding circuit. The data input wiring and signal input wiring for the same corresponding input holding circuit are equal in length.

To address this ground for rejection, Applicant incorporates by reference herein the same general comments set forth above for claim 8. In particular, just as the cited combination of reference/teachings does not show or suggest a "first wiring" and "second wiring", such teachings do not show or suggest a "data input wiring" and "m signal input wirings".

Amended Claim 20, which depends from claim 15, is believed to be separately patentable. Claim 20 recites that the memory controller further includes the m data input terminals and n signal input terminals being aligned with one another in a first direction and the m input holding circuits being aligned with one another in the first direction parallel to the data input terminals and signal input terminals.

To address this ground for rejection, Applicant incorporates the same general argument set forth above for claim 2. In particular, the alignment of such structures is not shown or suggested by the combination of references/teachings.

The present claims 1-21 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

November 13, 2006

Darryl G. Walker
Attorney
Reg. No. 43,232

Darryl G. Walker
WALKER & SAKO, LLP
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5314